48CH PROGRAMMABLE LOGIC MODULE
N-PL 101
HARDWARE MANUAL

Technoland Corporation

Corporate Headquarters
902-1 Tonogaya,Mizuho,Tokyo,Japan
Zip：190-1212
http://www.tcnland.co.jp

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1 Abstract

FEATURES

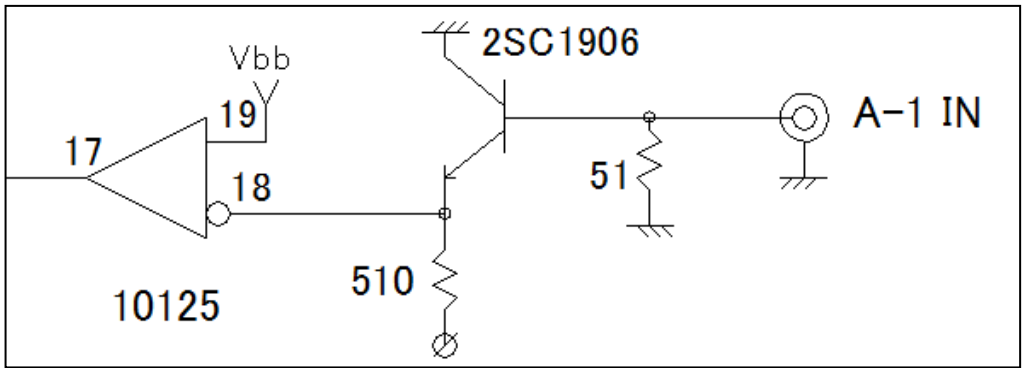
- Selectable Input / Output : 48CH
- Special Input : FAST NIM /1CH
- Input / Output Signal : FAST NIM
- Programmable Status LED : 4
- Available CPLD : MAX7000 Series (ALTERA)
- User Setting CPLD in a Socket : 84-Pin PLCC
- The Program is Loaded : Program Port (Rear Panel)

2 Product Description

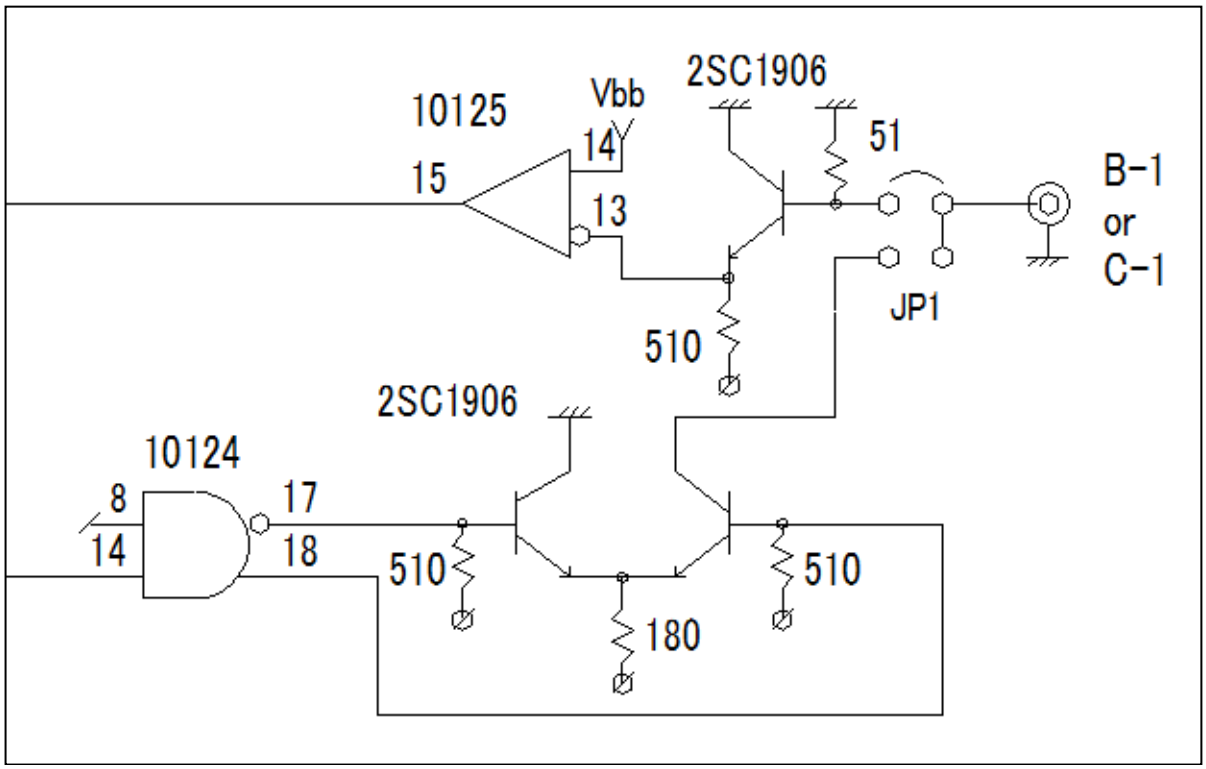
N-PL 101 is the module which can program the logic by a user freely. The port of 32 channels can choose inputs and outputs in one group in 4-channels. The user chooses input and the output by the setting of the jumper pin. The LED on the front panel displays the in/out state.
One special external input is connected to GCLK (PIN No.83) input of CPLD. The latch of input data can use this signal.
All input and output signal are FAST NIM signals.
This module has four LED for status indication. The user can program this indication by the logic (CPLD).
The write of logic data uses the 10-pin header of the rear panel.
The internal clock (48MHz) is connected to GCLK2 (PIN No.2) of CPLD.

3 Input / Output Characteristics

Number of Channel	: 48
Signal	: FAST NIM
Impedance	: 50Ω
Minimum Pulse Width	: 10ｎS
Connecter Type	: LEMO (ERA.00.250)
In / Out Select	: every 4-channel , used select jumper switches,
＊16channels of A-line	: Input only



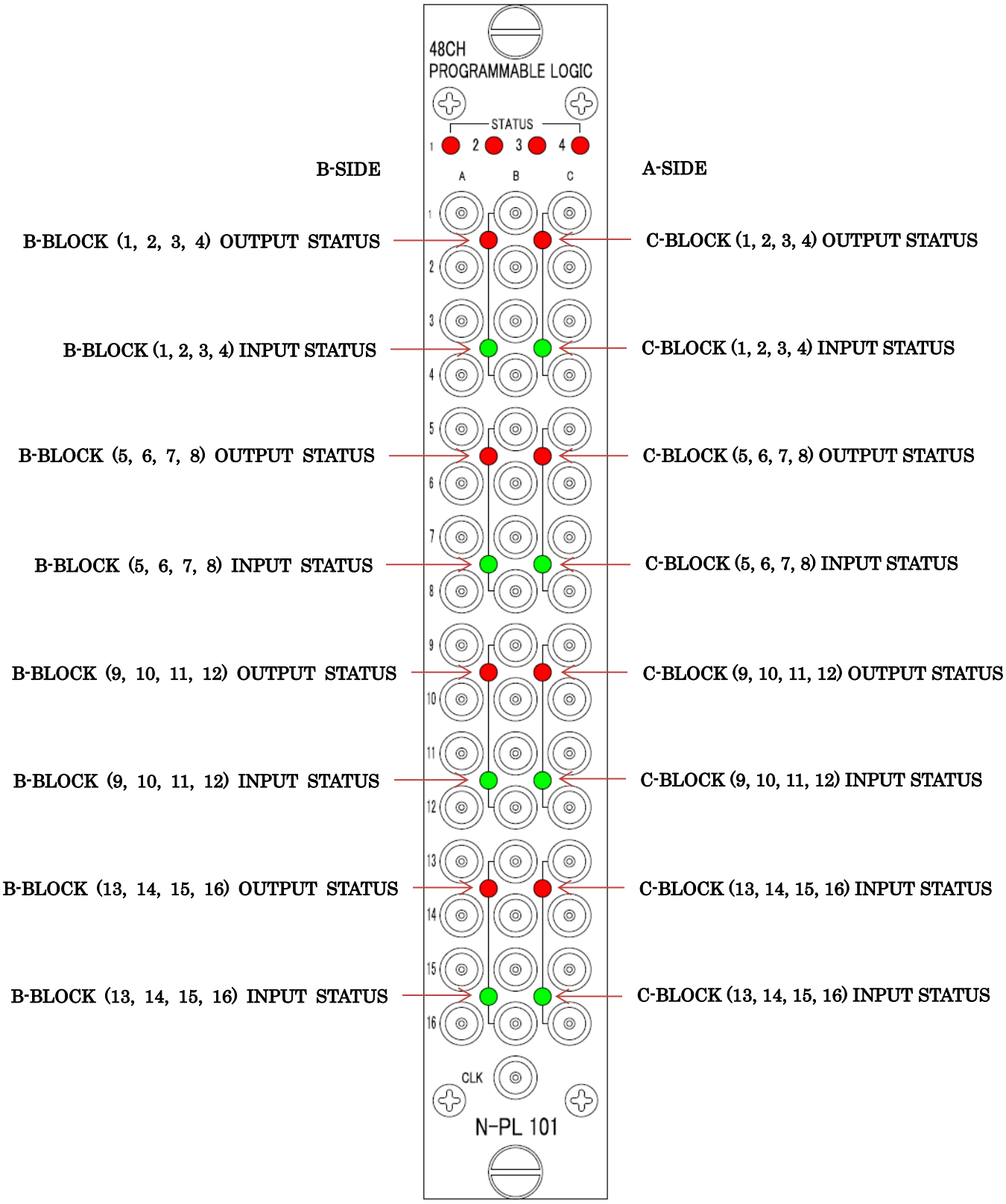
A-Line : Input Only



B or C-Line : Input / Output (JP -select)

4 Select Operation of the Input and Output

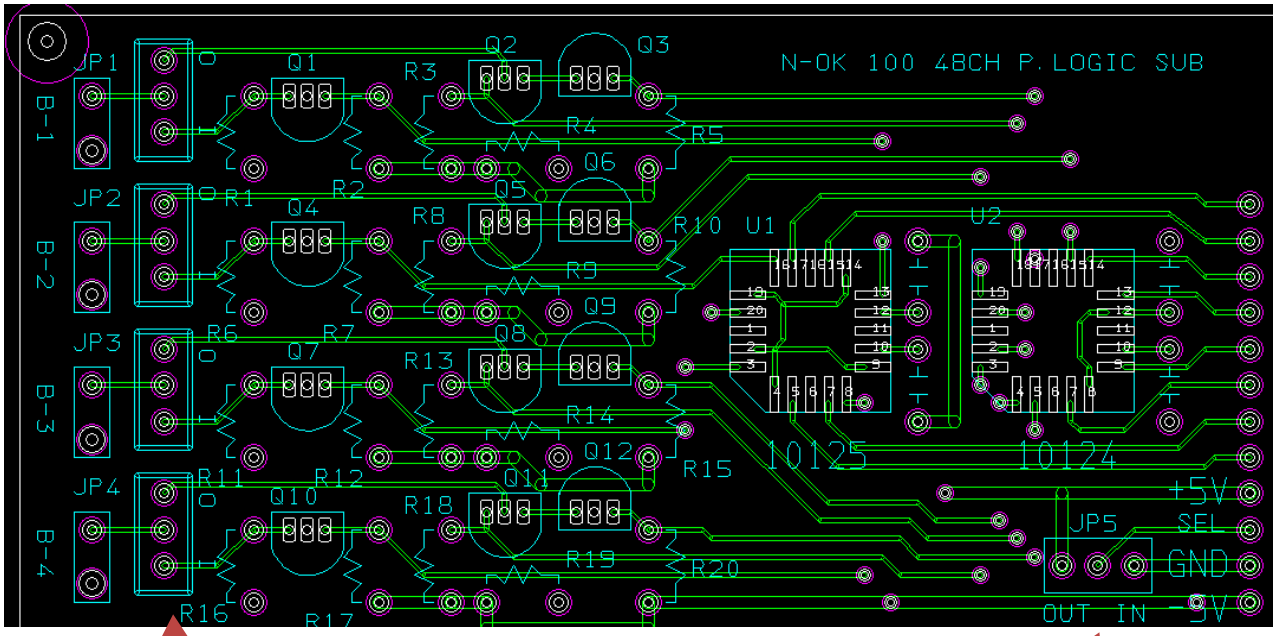
The A-side has the reshuffling JP -socket of 32-channels.
1- Division is constructed in 4-Channels.



4.1 Setting ofJP5

4.1.1 Select of INPUT/OUTPUT

Example : 1-Block (B-1～B-4), A-SIDE view



JP1,2,3,4 for INPUT (I) or OUTPUT(O)

Select for INPUT / OUTPUT

(1) The user must decide input or the output by JP5.
(2) Then, you set B and C (JP1, 2, 3, 4). This setting must make it the same as JP5.

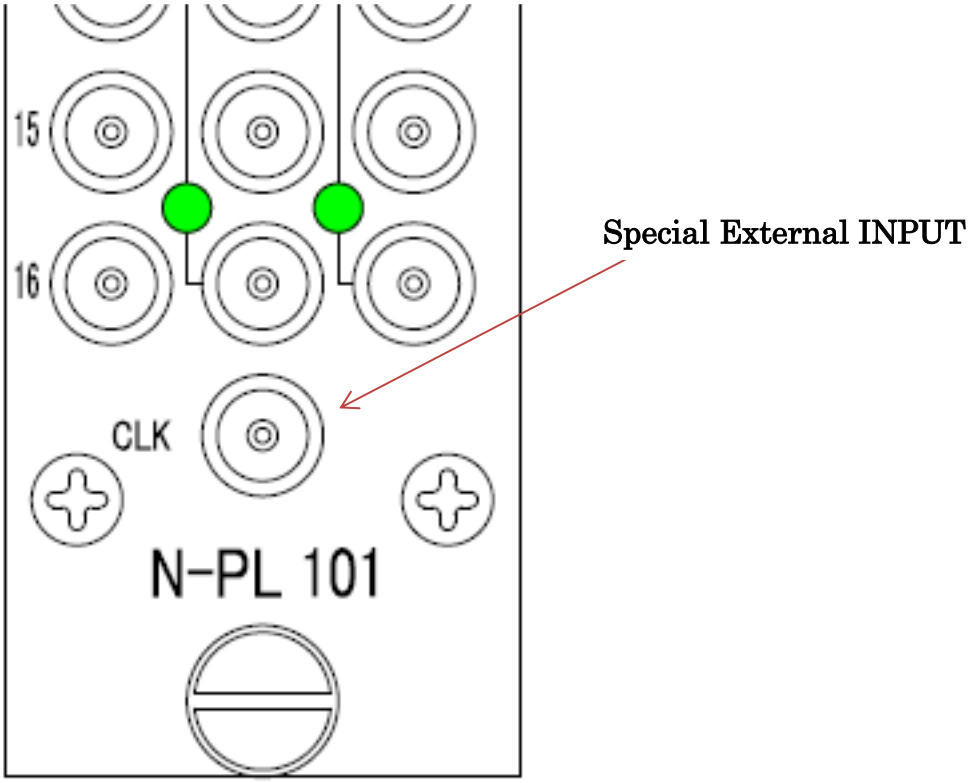
Example : In the case of INPUT-USE

JP5・・・IN
JP1・・・I
JP2・・・I
JP3・・・I
JP4・・・I

＊All Jumper must be IN(I) in this block. And green LED turns on. Red LED turns on if setting is the OUTPUT.

5 Special external input

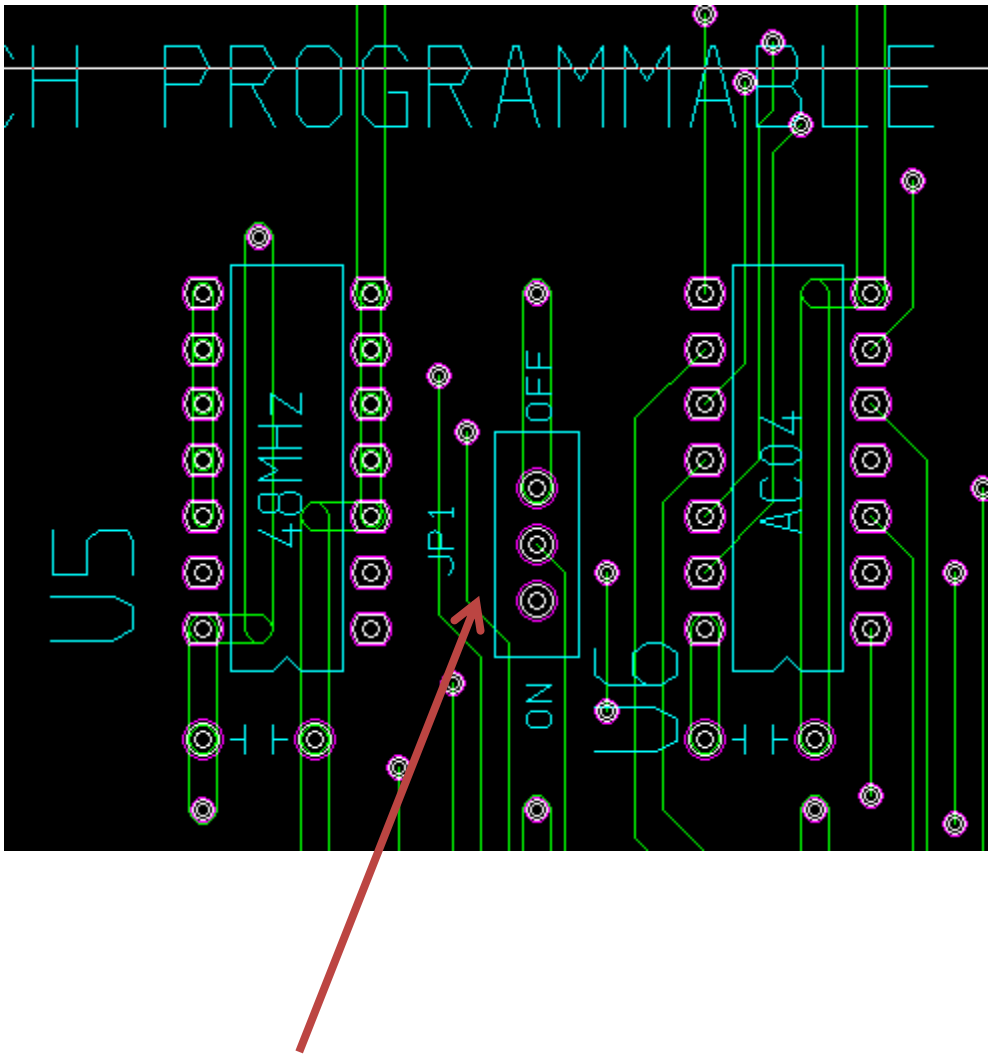
Number of Channels	: 1
Signal	: FAST NIM
Impedance	: 50 Ω
Minimum Pulse Width	: 10 n S
Maximum Rate	: 50MHz



6 About an Internal Clock

Frequency : 48MHz

This clock is connected to CPLD (GCLK PIN No.2). But the user does connection in JP1 of the main board. CPLD can in this way reduce the influence of the clock noise.
This JP1 is set in 'OFF' at the time of shipment. When you turn on this setting, please set JP1 of the B-side (main board) in 'ON'.



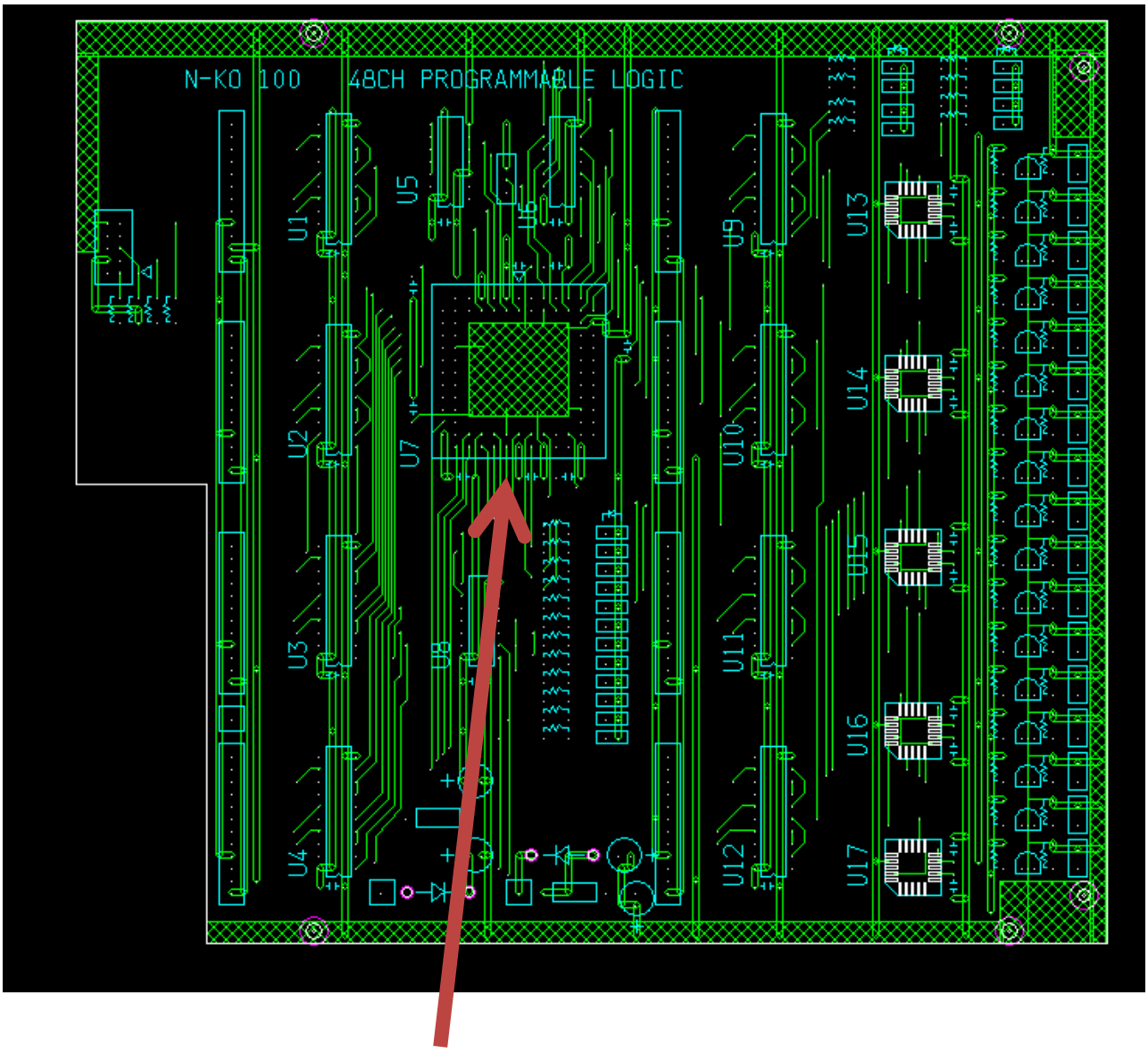
JP1 for "INTERNAL CLOCK"

7 Available CPLD

MAX7000 series : ALTERA

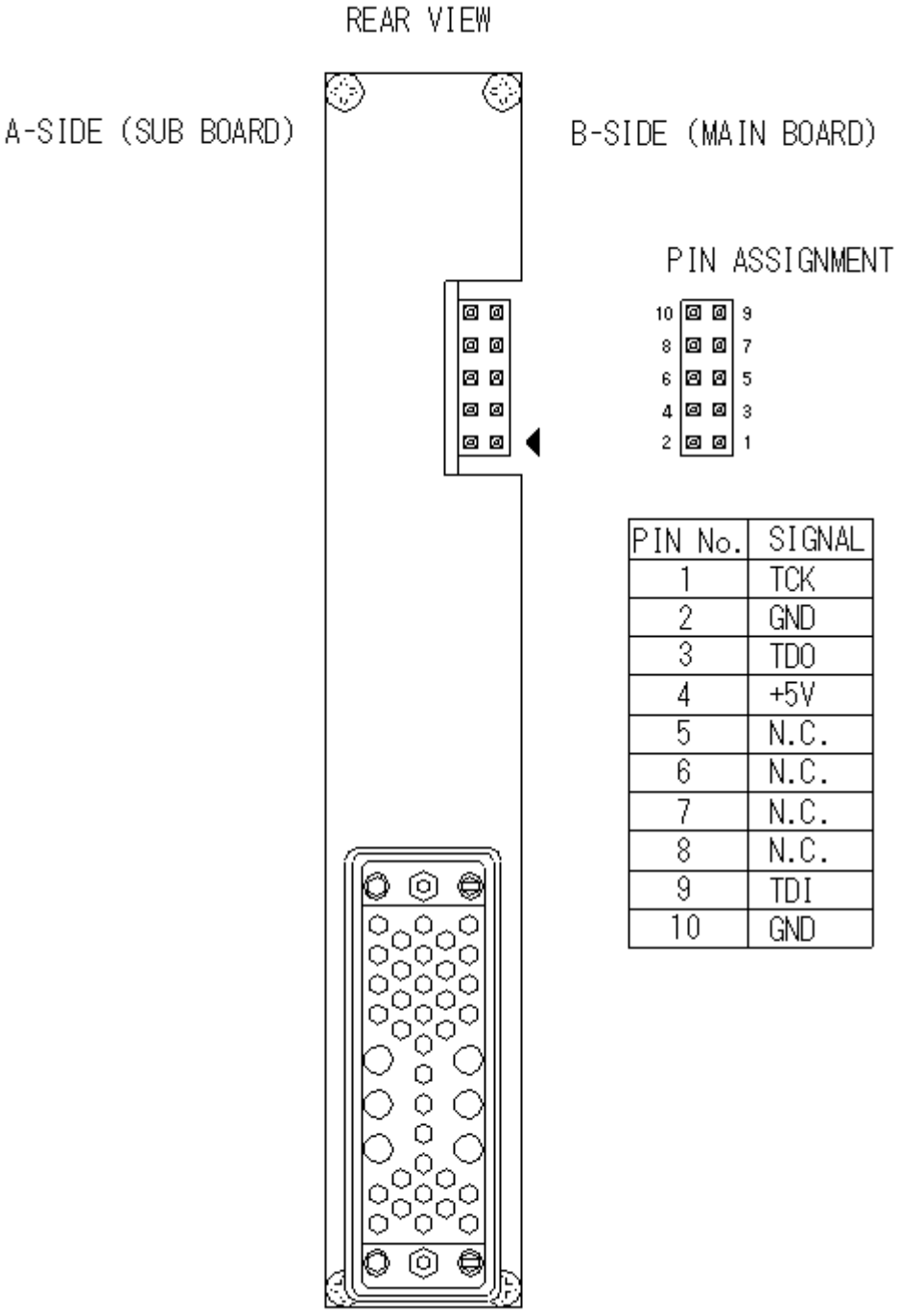
EPM7064S : The number of macrocells "64"
EPM7128S : The number of macrocells "128"

These CPLD is PLCC packages of 84PIN.
The user inserts CPLD in the IC socket (U7) of the main board (B-SIDE) and uses it.



"CPLD" inserts it in this socket.

8 About the input connector for programs



PIN No.	SIGNAL
1	TCK
2	GND
3	TDO
4	+5V
5	N.C.
6	N.C.
7	N.C.
8	N.C.
9	TDI
10	GND

The user writes in a program from this connector by “USB-BLASTER”.

9 Relations of the pins and the input / output of CPLD

LEMO-CONNECTOR “A” “B” “C”

IN	PIN No.	IN / OUT	PIN No.	IN / OUT	PIN No.
A-1	67	B-1	76	C-1	4
A-2	68	B-2	74	C-2	5
A-3	61	B-3	73	C-3	6
A-4	60	B-4	70	C-4	8
A-5	56	B-5	64	C-5	10
A-6	57	B-6	69	C-6	9
A-7	55	B-7	63	C-7	27
A-8	54	B-8	65	C-8	25
A-9	52	B-9	46	C-9	12
A-10	51	B-10	45	C-10	11
A-11	49	B-11	48	C-11	17
A-12	50	B-12	44	C-12	15
A-13	41	B-13	36	C-13	18
A-14	40	B-14	35	C-14	16
A-15	37	B-15	30	C-15	22
A-16	39	B-16	33	C-16	20

Another PIN

LED	PIN No.	CLOCK	PIN No.
Status-1	81	Internal	2
Status-2	80	External	83
Status-3	75		
Status-4	77		

＊Internal CLOCK : 48MHz
＊External CLOCK : Special external input